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9. Simatic Step 5 Timer Functions

Depending on which type of Siemens SIMATIC S5 PLC, all provide a certain number of times (e.g. the S5 115U has 128 timers, from T 0 to T 127), for which one word each (16 bits) is reserved in system memory.

9.1 Specifying the Time

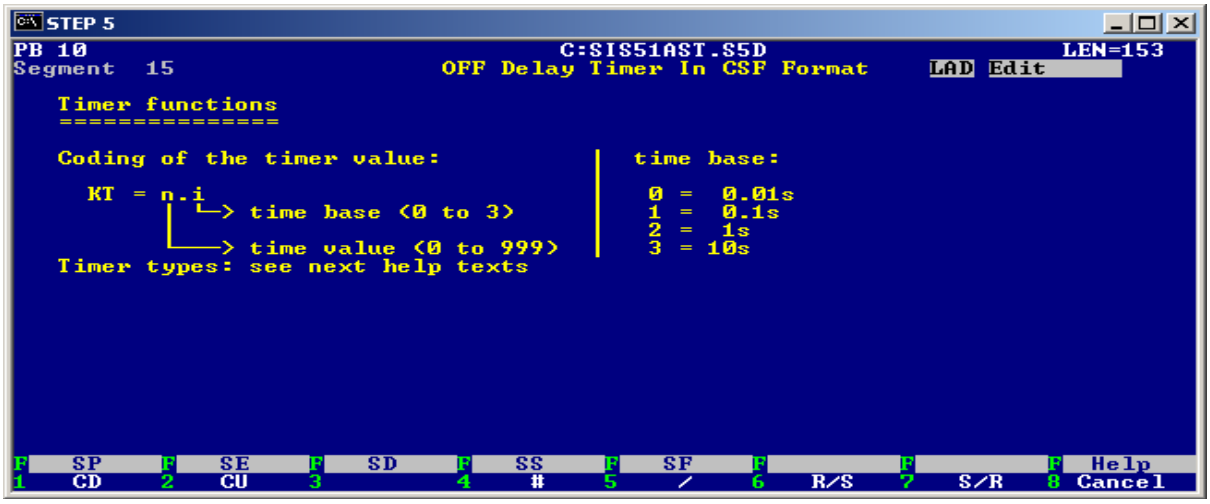
The time value **TV** of a timer can be specified in one of the following formats,:

- specified as a **CONSTANT** in the program (KT 432.1)
- entered as a **VARIABLE** value using an input word, dataword or flagword.

9.1.1 Structure of the time word

The time value consists of 3 decades and is specified in BCD code (1 to 999). The time word is 16 bits long and the time value occupies a maximum of 12 bits, starting from the right (bit 0 to bit 11). Bits 12 and 13 contain the time base (0 to 3). Bits 14 and 15 are irrelevant for specifying the time.

9.1.1.1 Specifying the Timer Base



SPECIFYING THE TIME BASE

9.1.1.2 Accuracy:

The accuracy of the timer is determined by the time base. The highest accuracy is obtained by specifying the time with the **SMALLEST TIME BASE** (in the example **KT 500.0**). The internal clock pulse is generated independently of the scan time. The user therefore has no influence on the position of the starting point within the internal clock pulse grid.

The time can therefore vary by one base unit depending on the position of the starting point.

The user defines the clock pulse rate by specifying the time base.

Example: A time of 5's (five seconds) can be specified with different time bases:

KT 005.2
KT 050.1
KT 500.0

Example:

	Accuracy		Error
KT 500.0	500 x 0.1's	49.9's ---50's	max 0.1's
KT 050.2	50 x 1's	49's---50's	max 1's
KT 005.3	5 x 10's	40's---50's	max 10's

Note: It is therefore advisable to select the smallest possible time base if high accuracy is important.

9.2 Programming of Timers in Step 5

There are three options to program any Timer using Step 5 and they are as follows,

- Ladder (Ladder Logic)
- STL (Statement List)
- CSF (Continuous System Flow)

Using Step 5 there are five different types of timer as follows,

- Pulse (SP)
- Extended Pulse (SE)
- On Delay (SD)
- Stored On Delay (SS)
- OFF Delay (SF)

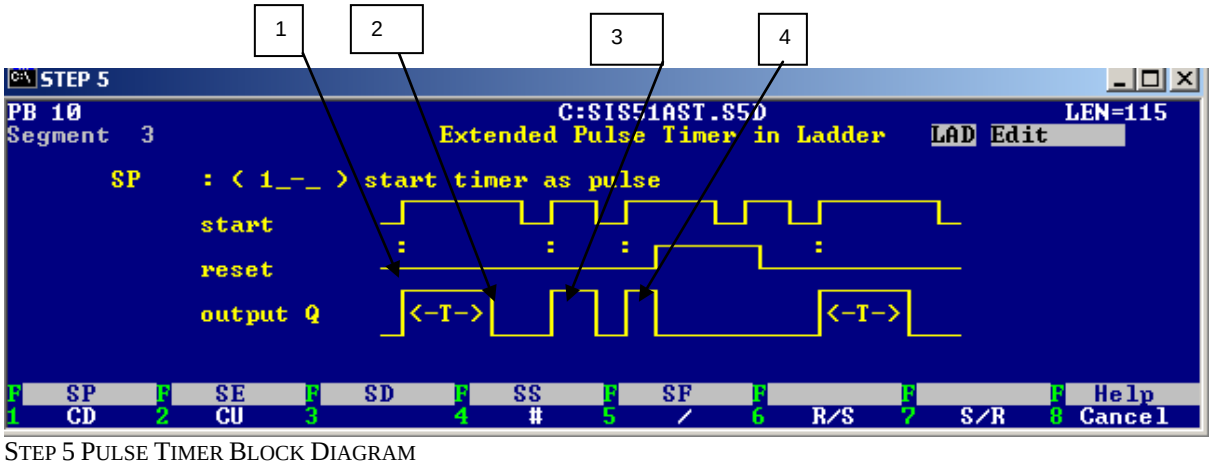
9.2.1 Pulse Timer (SP)

A pulse timer is used to provide a pulse when a rising edge is received at the input. The output of the timer started as a pulse (rising edge at the Start input) has the signal state '1' when the timer has been started (1).

Note: The output is reset when:

- the programmed time has elapsed or
- the Start signal is reset to '0' or
- the Reset input of the timer has the signal state '1'.

Below is a detail diagram of a Pulse Timer (SP),

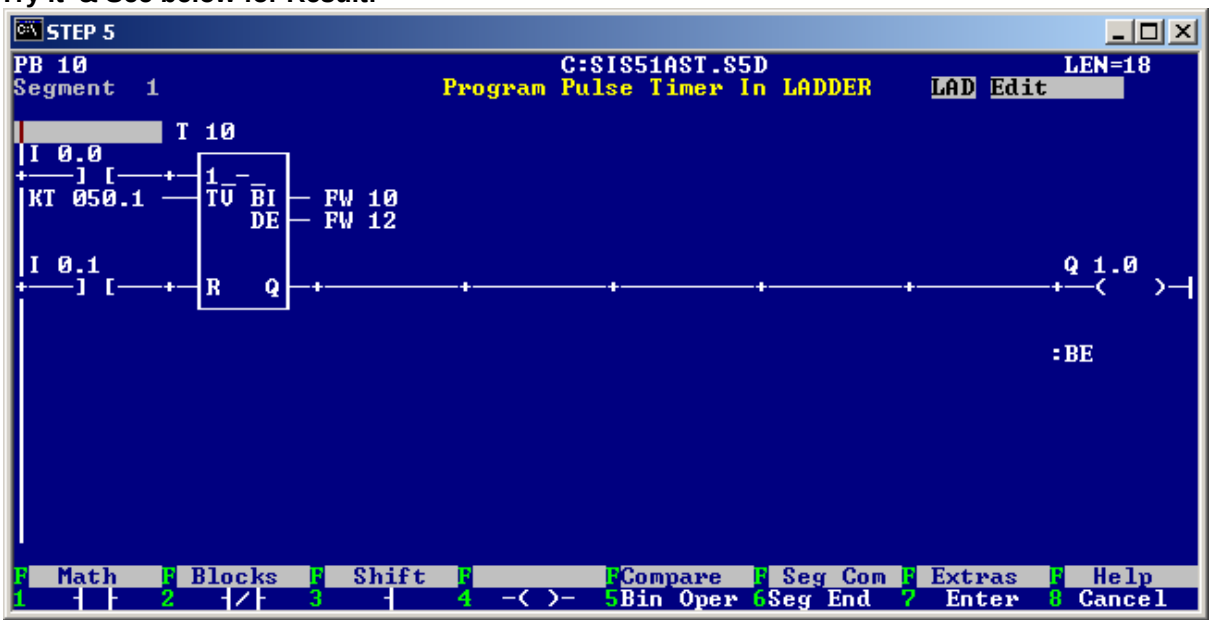


STEP 5 PULSE TIMER BLOCK DIAGRAM

9.2.2 Exercise Create a Pulse Timer (SP) using Ladder Logic

Create and program a Pulse Timer (SP) using Ladder Logic in Program Block 10 Segment 1 (PB10),

Try It & See below for Result:

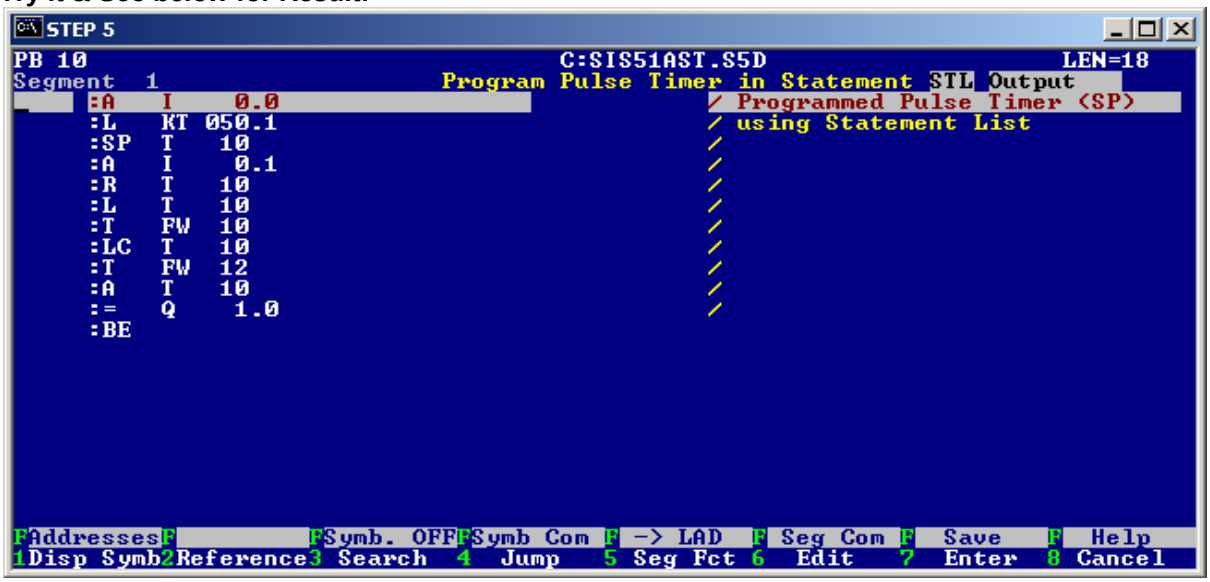


STEP 5 PULSE TIMER (SP) IN LADDER LOGIC

9.2.3 Exercise Create a Pulse Timer (SP) using Statement List

Create and program a Pulse Timer (SP) using statement List in Program Block 10 Segment 2 (PB10),

Try It & See below for Result:

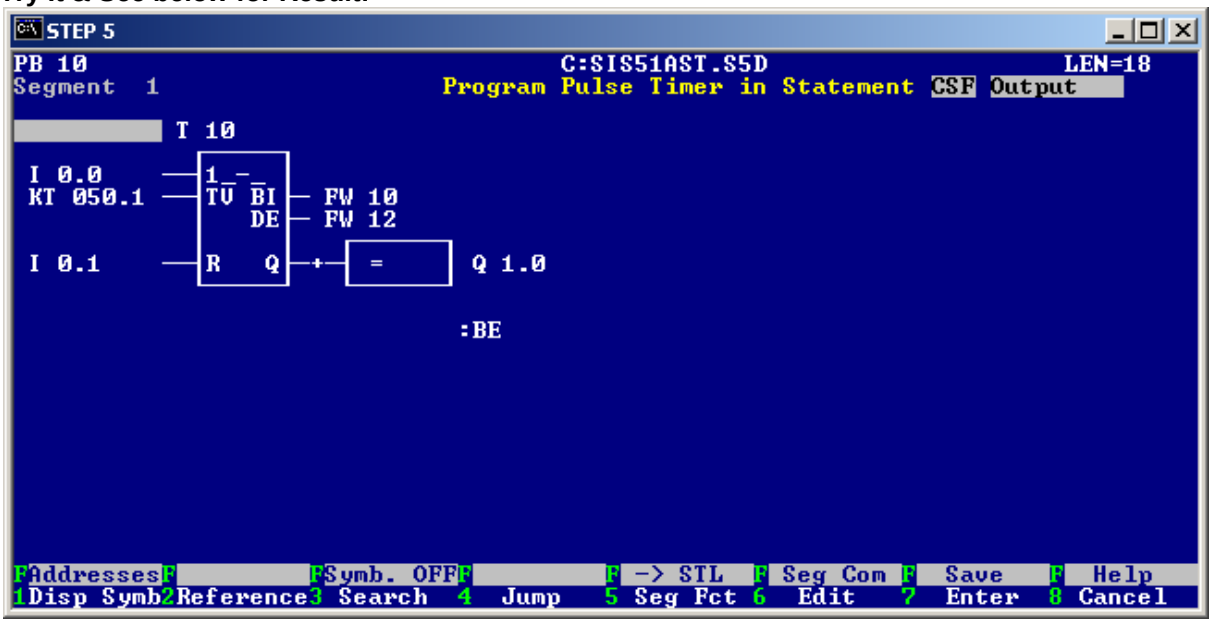


STEP 5 PULSE TIMER (SP) IN STATEMENT LIST

9.2.4 Exercise Create a Pulse Timer (SP) using CSF Format

Create and program a Pulse Timer (SP) using CSF Format in Program Block 10 Segment 3 (PB10),

Try It & See below for Result:



STEP 5 PULSE TIMER (SP) IN CSF FORMAT

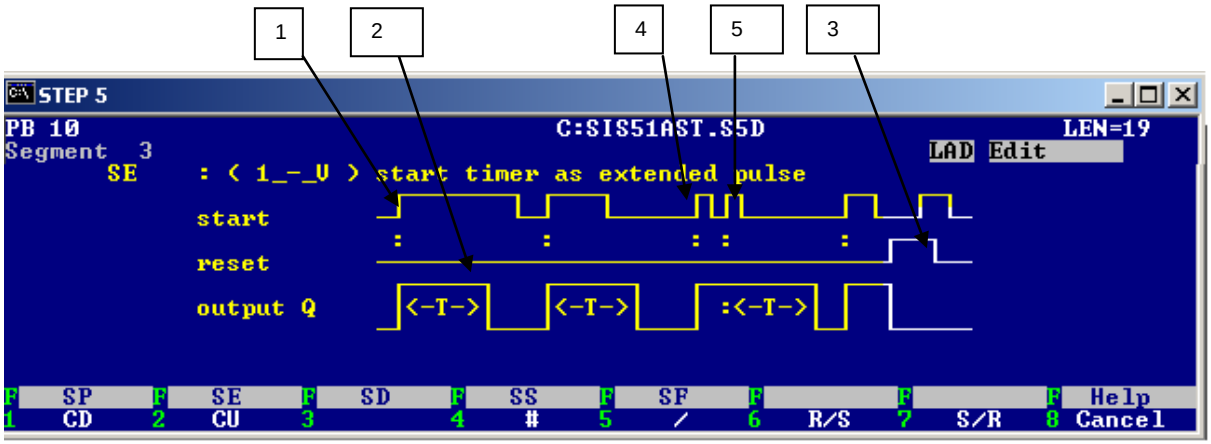
9.2.5 Extended Pulse Timer (SE)

An Extended Pulse timer is used to provide an extended pulse when a rising edge is received at the timers input. The output of a timer started as an extended pulse is set to '1' when the timer has been started (rising edge at the Start input).

Note: The output is reset when:

- the specified time has elapsed (2) or
- the Reset input of the timer function is activated (3).
- Deactivating the Start input whilst the timer is running does **not** cause the output to be reset (latching) (4). The timer continues to run !
- If the signal at the Start input changes from '0' to '1' again whilst the timer is running, the timer is started again ("re-triggered") (5).

Below is a detail diagram of a Extended Pulse Timer (SE),

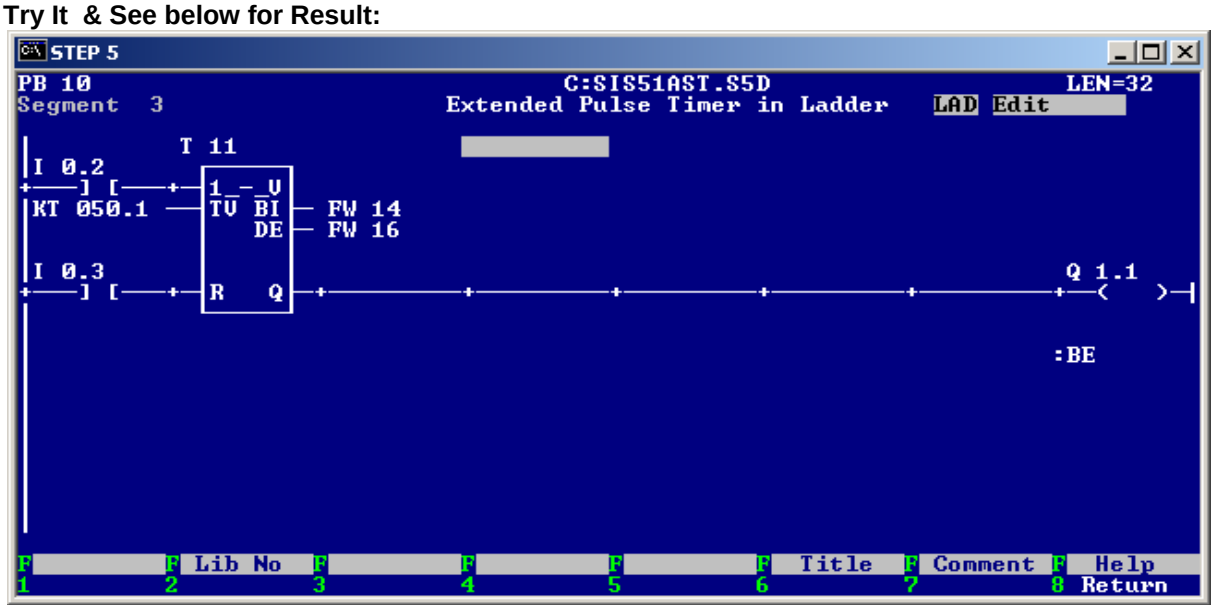


STEP 5 EXTENDED PULSE TIMER BLOCK DIAGRAM

9.2.6 Exercise Create an Extended Pulse Timer (SE) Using Ladder Logic

Create and program an Extended Pulse Timer (SE) using Ladder Logic in Program Block 10 Segment 4 (PB10),

Try It & See below for Result:

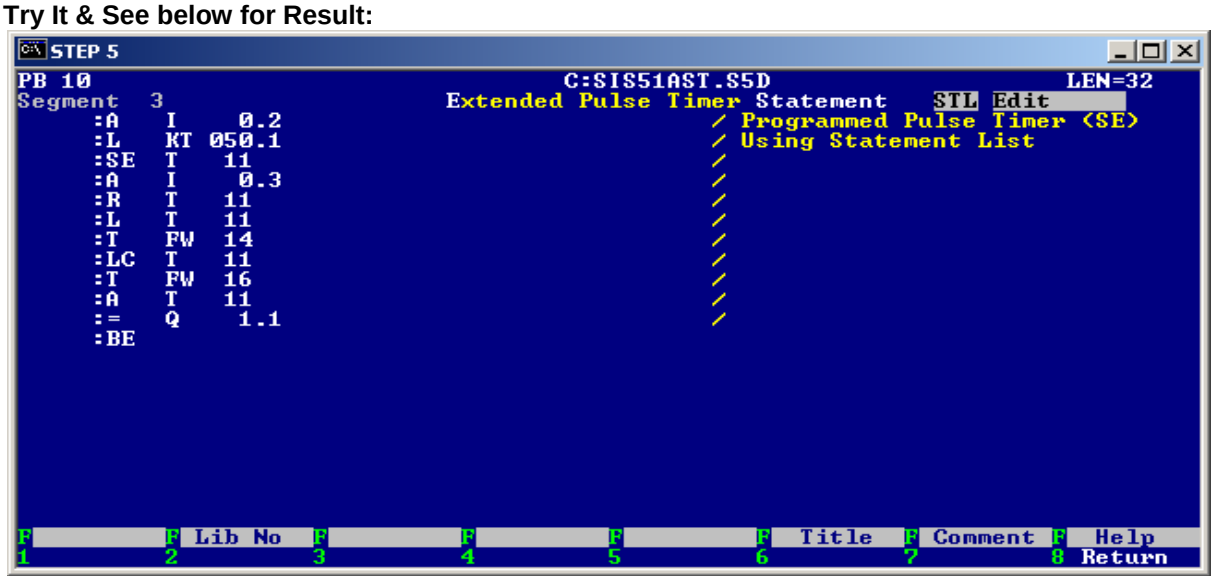


STEP 5 EXTENDED PULSE TIMER (SE) IN LADDER LOGIC

9.2.7 Exercise Create an Extended Pulse Timer (SE) using Statement List

Create and program an Extended Pulse Timer (SE) using Statement List in Program Block 10 Segment 5 (PB10),

Try It & See below for Result:

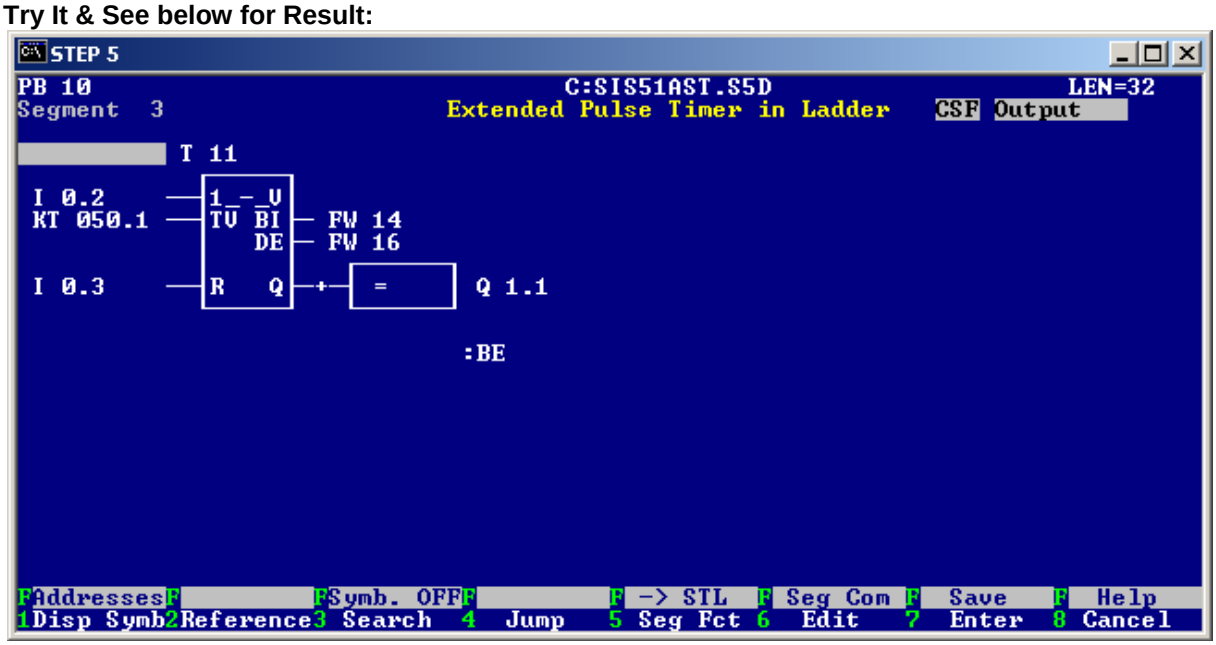


STEP 5 EXTENDED PULSE TIMER (SE) IN STATEMENT LIST

9.2.8 Exercise Create an Extended Pulse Timer (SE) using CSF Format

Create and program an Extended Pulse Timer (SE) using CSF Format in Program Block 10 Segment 6 (PB10),

Try It & See below for Result:



STEP 5 EXTENDED PULSE TIMER (SE) IN CSF FORMAT

9.2.9 ON Delay Timer (SD)

An On Delay timer is started when a rising edge is received at the timers input. The output of a timer started as an ON delay (rising edge at the Start input) only assumes the signal state '1' after the timer has been started when:

- the programmed time has elapsed and
- the Start input still has RLO '1' (1).

Activating the Start input therefore causes output Q to be activated after the specified time.

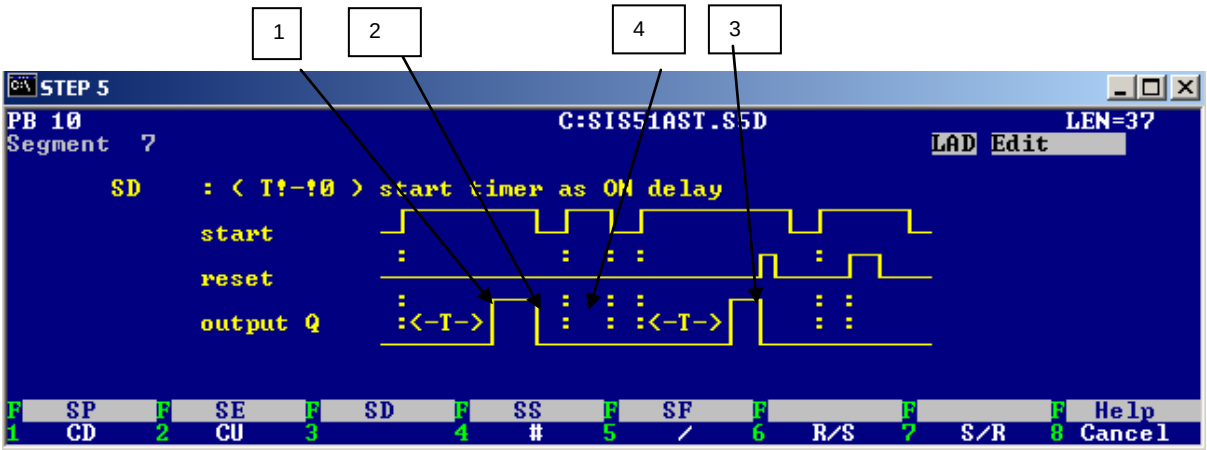
Note: The output is reset when:

- the Start input is deactivated (2) or
- the Reset input has the signal state '1' (3).

Deactivating the Start input only stops the counter (the time recorded so far is retained). When the signal at the Start input changes again (from '0' to '1') the timer starts again for the full time. The output is not activated until the timer expires (4).

As soon as the Reset input has the signal state '1', the contents of the timer are reset to '0' (4). The timer remains stopped even when the Reset input is no longer set (it is only started by a rising edge at the Start input).

Below is a detail diagram of a On Delay Timer (SD),

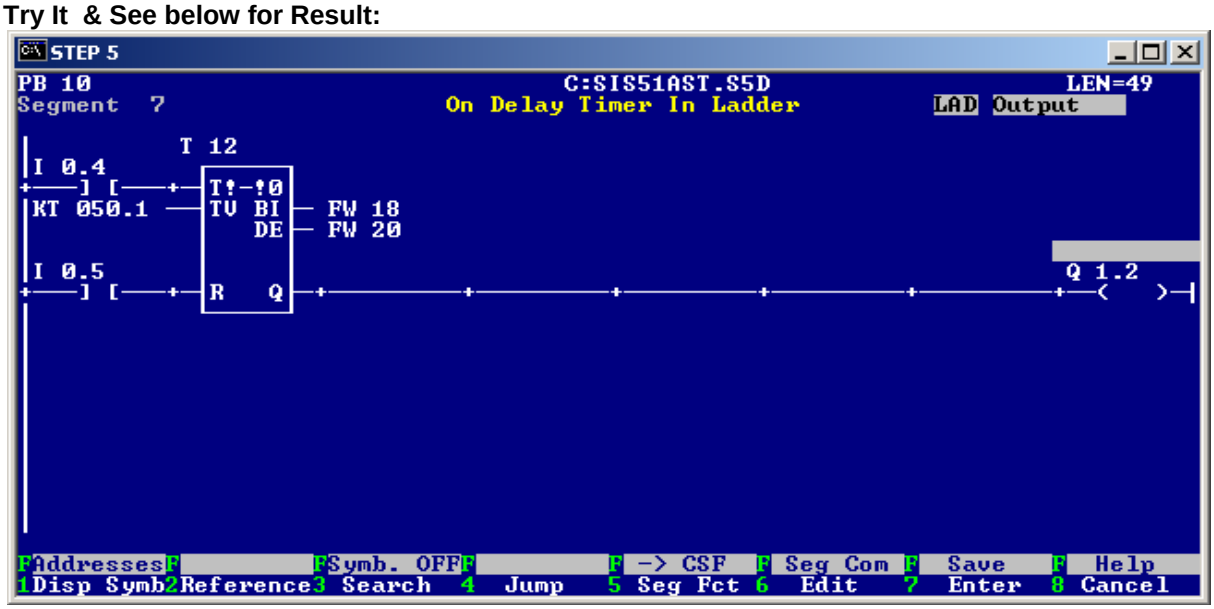


STEP 5 ON DELAY TIMER BLOCK DIAGRAM

9.2.10 Exercise Create an On Delay Timer (SD) Using Ladder Logic

Create and program an On Delay Timer (SD) using Ladder Logic in Program Block 10 Segment 7 (PB10),

Try It & See below for Result:

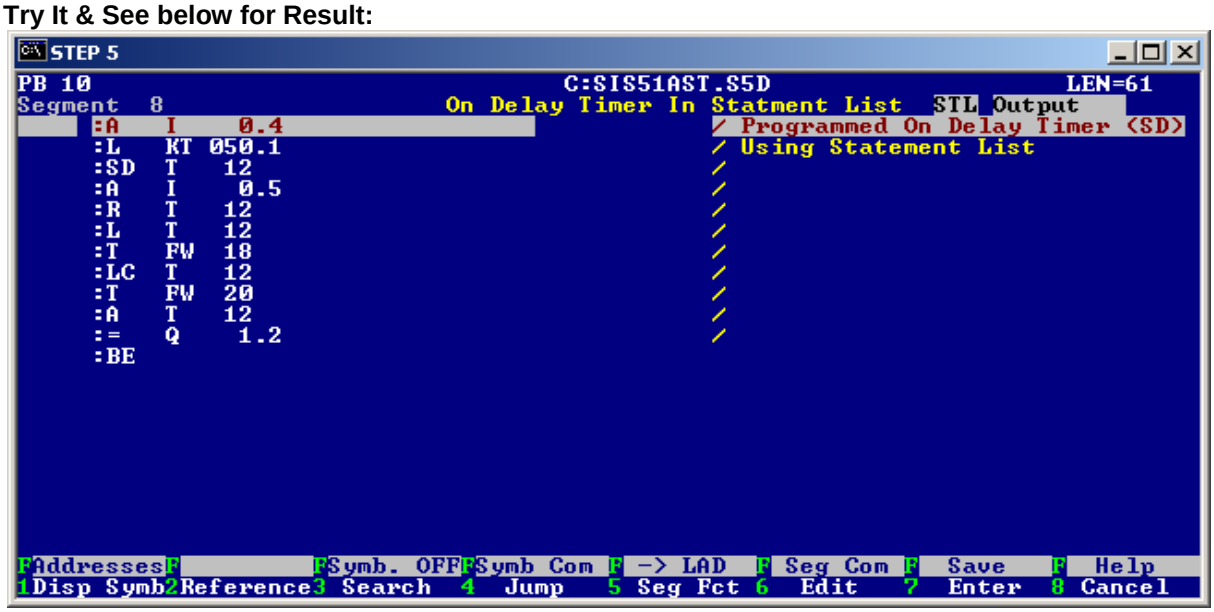


STEP 5 ON DELAY TIMER (SD) IN LADDER LOGIC

9.2.11 Exercise Create an On Delay Timer (SD) using Statement List

Create and program an On Delay Timer (SD) using Statement List in Program Block 10 Segment 8 (PB10),

Try It & See below for Result:

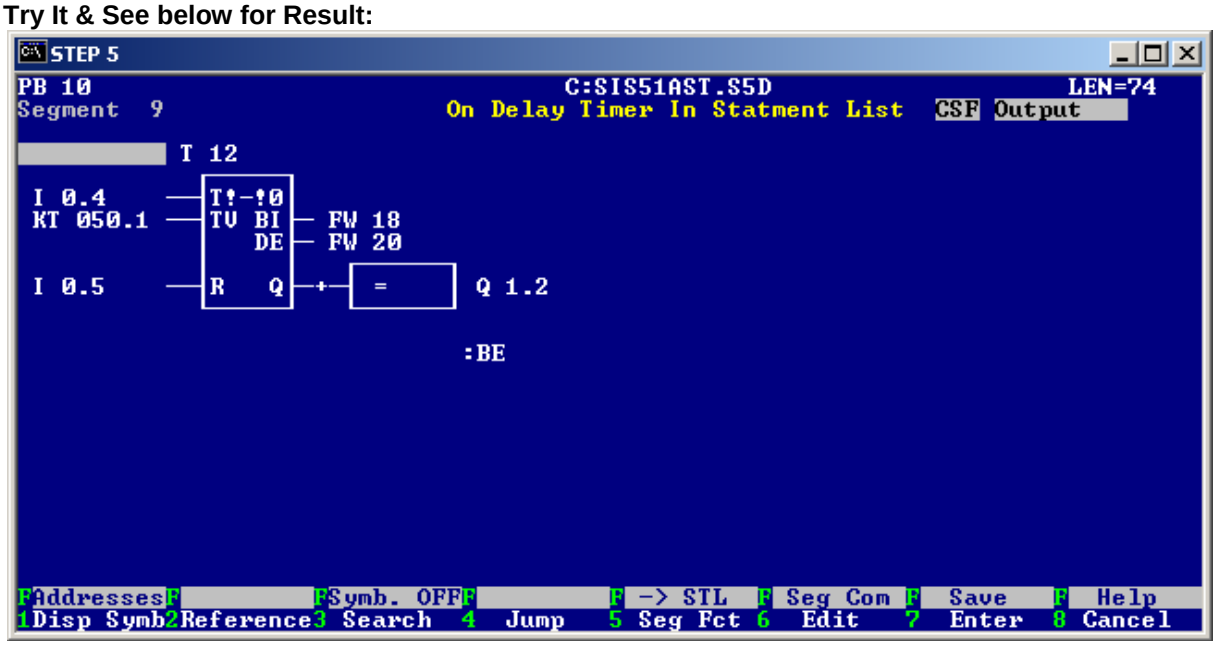


STEP 5 ON DELAY TIMER (SD) IN STATEMENT LIST

9.2.12 Exercise Create an On Delay Timer (SD) using CSF Format

Create and program an On Delay Timer (SD) using CSF Format in Program Block 10 Segment 9 (PB10),

Try It & See below for Result:



STEP 5 ON DELAY TIMER (SD) IN CSF FORMAT

9.2.13 Stored ON Delay Timer (SD)

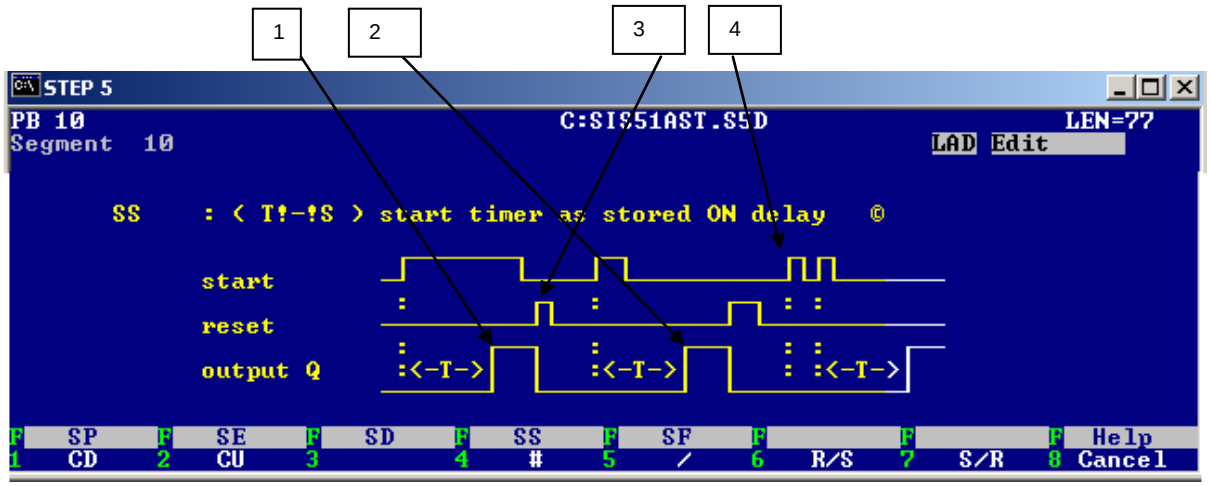
A Stored On Delay timer is started when a rising edge is received at the timers input. The output of a timer started as a Stored ON delay (rising edge at the Start input) only assumes the signal state '1' after the timers programmed time has elapsed.

Only a short pulse is required to start the timer. The Start instruction is stored (latching) (2).

Note: The output can only be reset with the Reset input (3).

If another Start instruction is given whilst the timer is running, the full time loaded again ("re-triggering") (4).

Below is a detail diagram of a Stored On Delay Timer (SS),

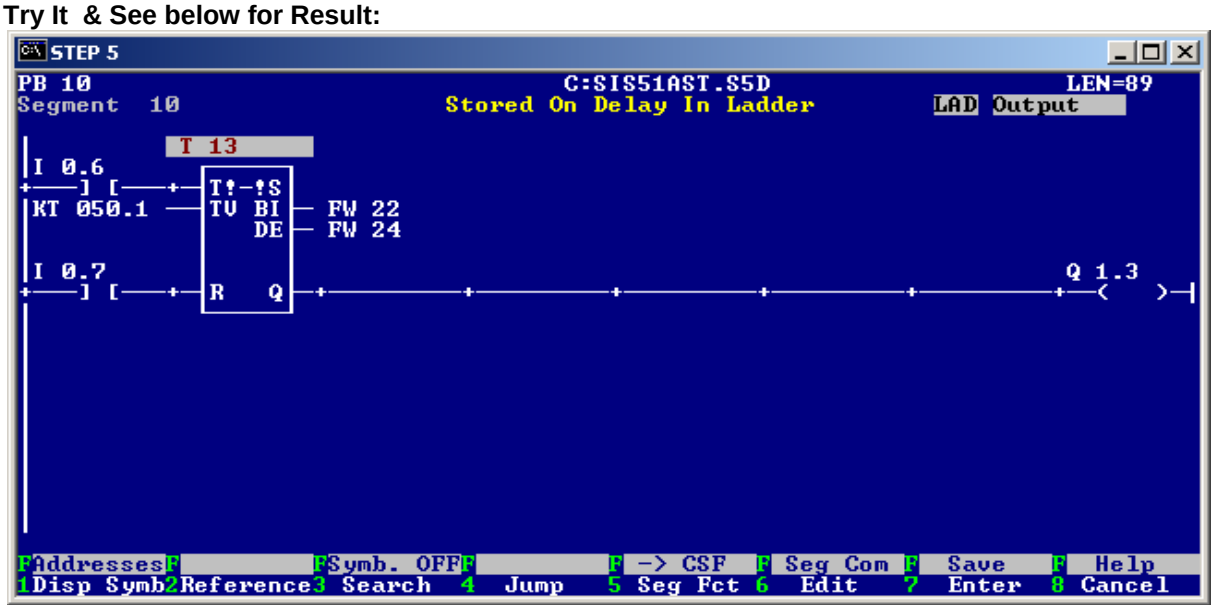


STEP 5 STORED ON DELAY TIMER BLOCK DIAGRAM

9.2.14 Exercise Create a Stored On Delay Timer (SS) Using Ladder Logic

Create and program a Stored On Delay Timer (SS) using Ladder Logic in Program Block 10 Segment 10 (PB10),

Try It & See below for Result:

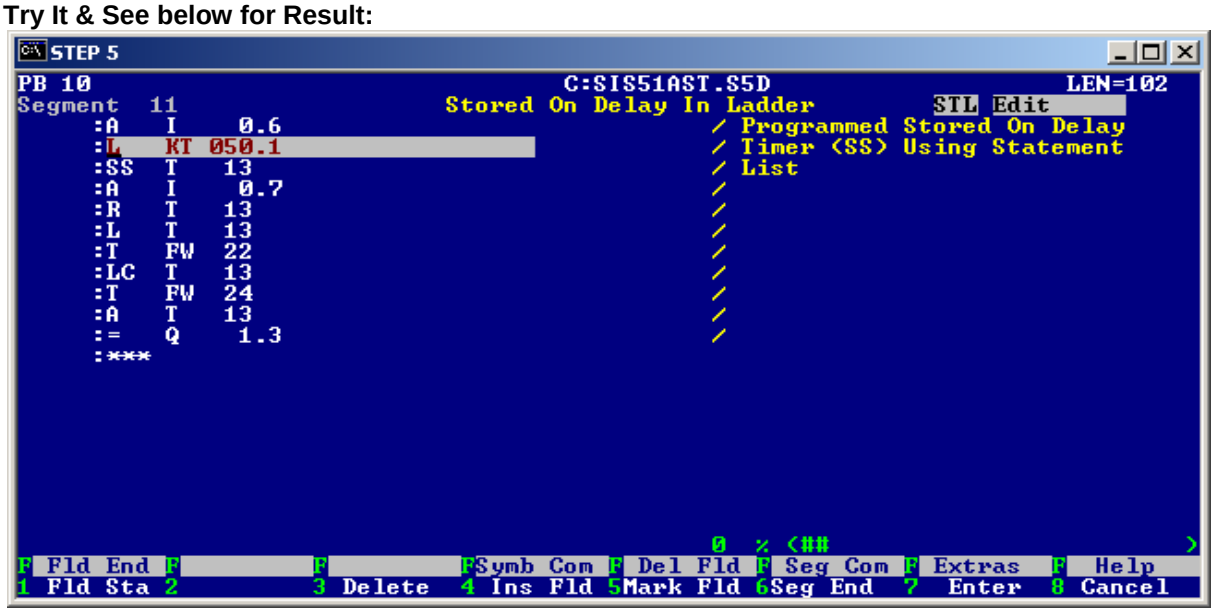


STEP 5 STORED ON DELAY TIMER (SS) IN LADDER LOGIC

9.2.15 Exercise Create a Stored On Delay Timer (SS) using Statement List

Create and program a Stored On Delay Timer (SS) using Statement List in Program Block 10 Segment 11 (PB10),

Try It & See below for Result:

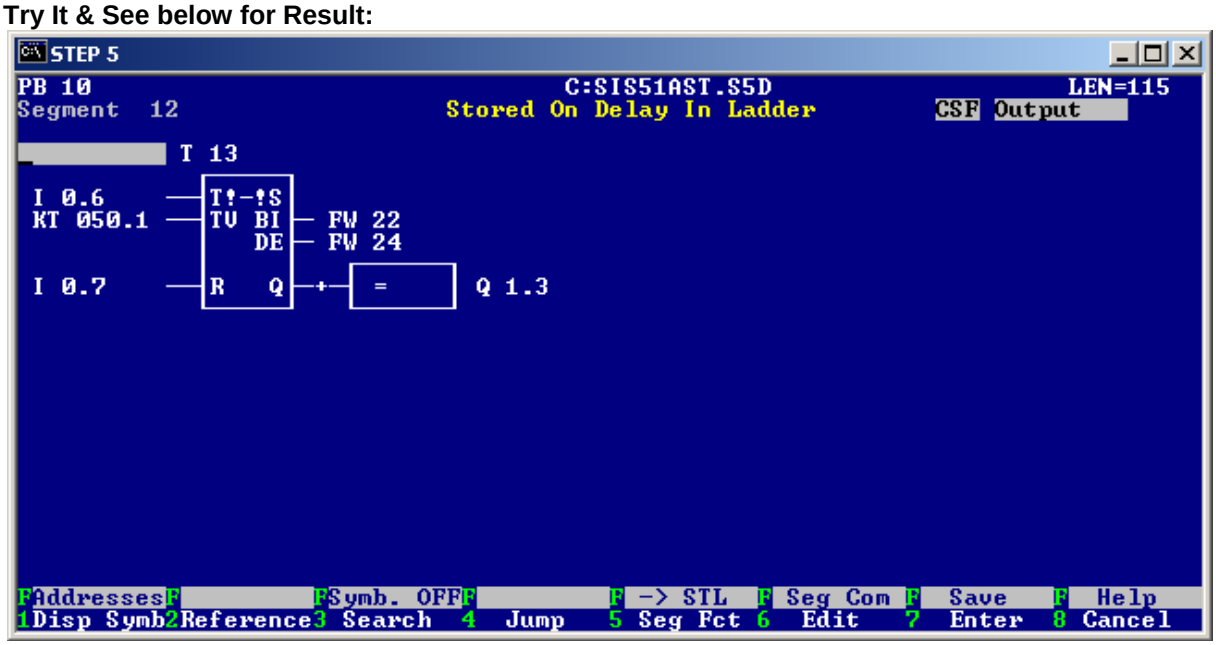


STEP 5 STORED ON DELAY TIMER (SS) IN STATEMENT LIST

9.2.16 Exercise Create a Stored On Delay Timer (SS) using CSF Format

Create and program a Stored On Delay Timer (SS) using CSF Format in Program Block 10 Segment 12 (PB10),

Try It & See below for Result:



STEP 5 STORED ON DELAY TIMER (SS) IN CSF FORMAT

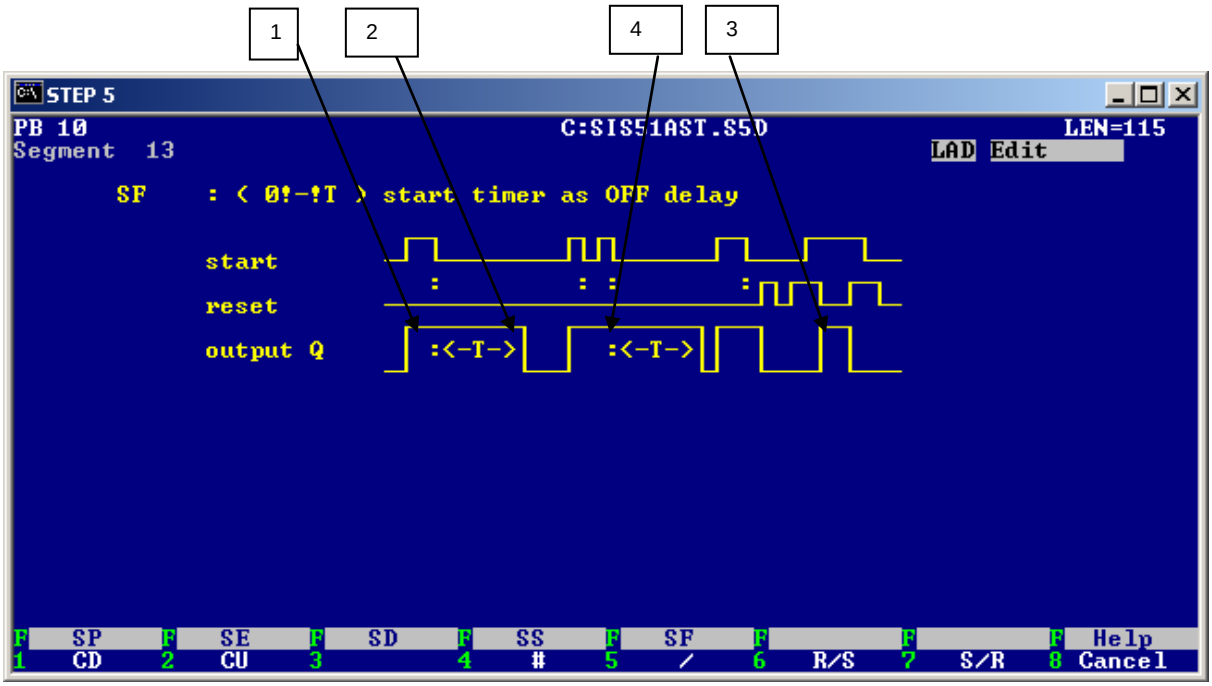
9.2.17 OFF Delay Timer (SF)

A Stored Off Delay timer is started when the Start input is deactivated (signal change from '1' to '0', **falling edge)** is received at the timers input. The output of a timer started as an Off Delay (falling edge at the Start input) assumes the signal state '1' immediately.

Note: The output can only be reset when

- When the programmed time has expired (2). Deactivating the Start input therefore causes the output to be deactivated after the specified time.
- The Reset input has the signal state '1' (3).
- The start input is re-activated and de-activated whilst the timer is running. The timer stops and starts again from the beginning when the Start input is deactivated again (4).
- If both the Start and Reset inputs of the timer have the signal state '1', the output of the timer is not set until the dominant Reset input is deactivated (5). However, the timer does not start until there is a falling edge at the Start input.

Below is a detail diagram of a Stored On Delay Timer (SS),

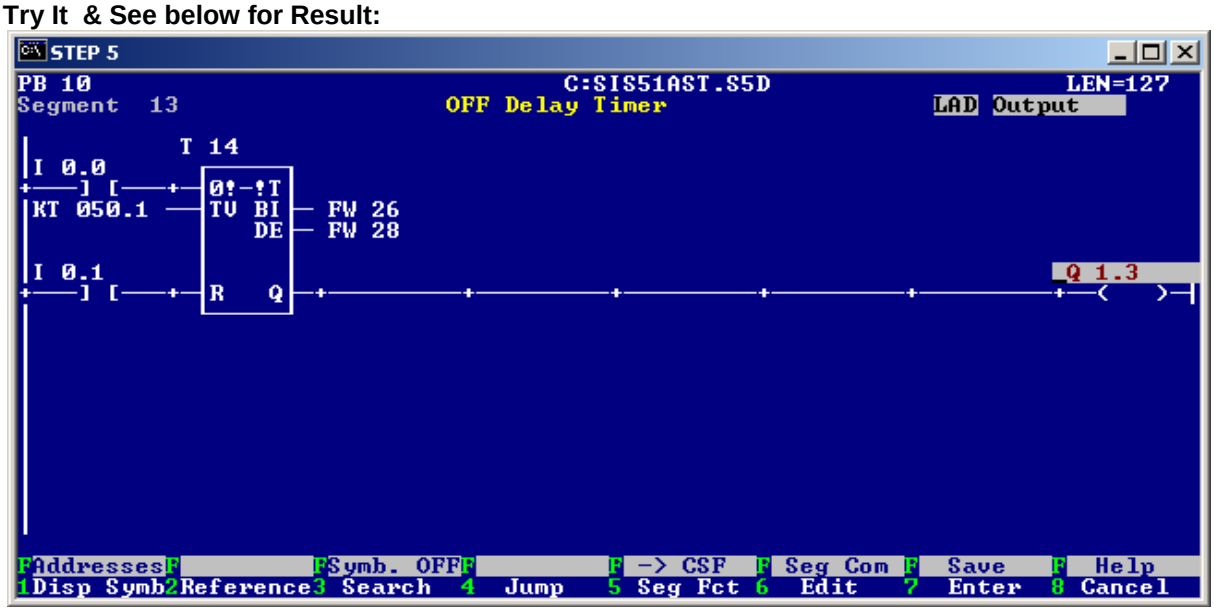


STEP 5 OFF DELAY TIMER BLOCK DIAGRAM

9.2.18 Exercise Create an OFF Delay Timer (SF) Using Ladder Logic

Create and program an OFF Delay Timer (SF) using Ladder Logic in Program Block 10 Segment 13 (PB10),

Try It & See below for Result:

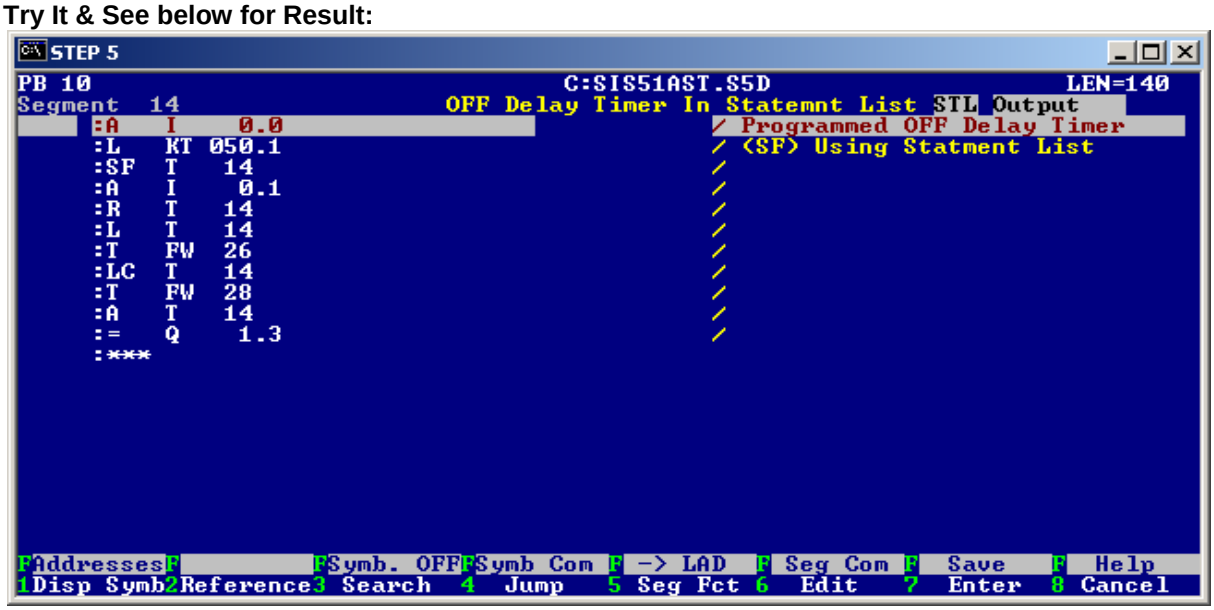


STEP 5 OFF DELAY TIMER (SF) IN LADDER LOGIC

9.2.19 Exercise Create a OFF Delay Timer (SF) using Statement List

Create and program an OFF Delay Timer (SF) using Statement List in Program Block 10 Segment 14 (PB10),

Try It & See below for Result:

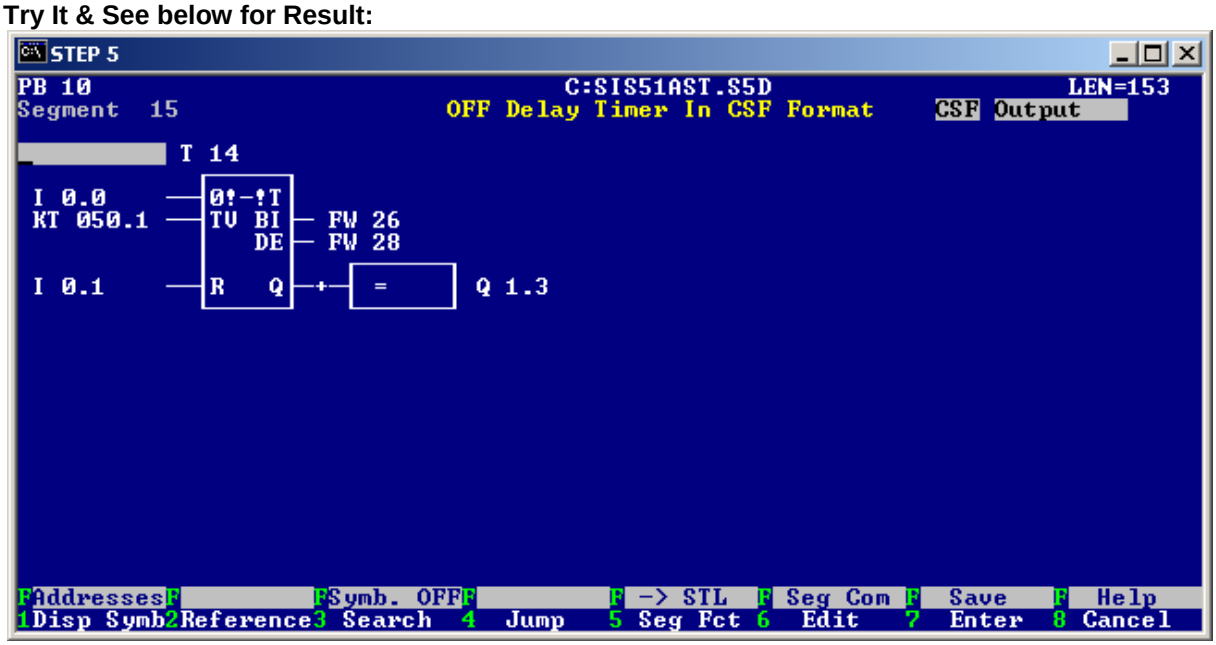


STEP 5 OFF DELAY TIMER (SF) IN STATEMENT LIST

9.2.20 Exercise Create an OFF Delay Timer (SF) using CSF Format

Create and program an OFF Delay Timer (SF) using CSF Format in Program Block 10 Segment 15 (PB10),

Try It & See below for Result:



STEP 5 OFF DELAY TIMER (SF) IN CSF FORMAT

9.3 Check What You Learnt in This Chapter

I Know:

⇒ How to specify time value.

⇒ How the structure of time word is made up.

⇒ How a Pulse Timer operates.

⇒ How a Extended Pulse Timer operates.

⇒ How a On Delay Timer operates.

⇒ How a Stored On Delay Timer operates.

⇒ How a OFF Delay Timer operates

9.4 I Can:

⇒ Program a Pulse Timer in Ladder, Statement or CSF Format.

⇒ Program a Extended Pulse Timer in Ladder, Statement or CSF Format.

⇒ Program a On Delay Timer in Ladder, Statement or CSF Format.

⇒ Program a Stored On Delay Timer in Ladder, Statement or CSF Format.

⇒ Program a OFF Delay Timer in Ladder, Statement or CSF Format.